ELECTRICAL ENGINEERING SEMINARS

كلية الهندسة
College of Engineering
QATAR UNIVERSITY جامعة قطر

The Department of Electrical Engineering cordially invites you to a seminar on

Reconfigurable Multi-Processor System-on-Chip Architectures in Intelligent Transportation Systems

By

Prof. Smail Niar

Date: Sunday, December 16, 2012

Time: 11:00am to 12:00pm

Venue: Male Engineering Building G - 209

Abstract

Traditionally, performance improvements have been achieved through increasing the clock frequency of the processors as faster transistors have been provided. However, the impact of power consumption, on system's reliability and cooling limited employing those techniques for further performance improvements. Two ways for increasing energy efficiency in embedded and communicating systems and for exploiting billions of transistors on a single chip are by the use of Multiprocessor Systems-on-Chip (MPSoC) or many core architectures in one side and customized-reconfigurable hardware components in the other side.

The combination or hybridization of these 2 techniques guarantees application-functional requirements and time-to-market while reducing power and energy consumption. During the last few years, the utilization of hardware accelerator, in the form of configurable hardware (namely FPGA) and the use of graphics processing units for accelerating general-purpose applications (the so-called GPGPU) has been advocated by several research projects and chipmakers. The new Xilinx Zynq 7000 and ARM Cortex A15-Mali are examples of such hybrid systems.

During the seminar, I will present our approach for the design of reconfigurable hybrid MPSoC FPGA-based architectures and its application for Intelligent Transportation Systems and Driver Assistant Systems (DAS).

I will explore the use of dynamic and partial reconfiguration to modify the architecture of FPGA. The purpose is to dynamically and automatically tune the MPSoC architecture to match the characteristics of the operational environment. Finally, an outlook on further key research issues in communicating embedded systems design to support the future "secured and mobile society" will be discussed.

Speaker's Bio:

Pr. Smail Niar (University of Valenciennes & CNRS, France) received his PhD in computer Engineering from the University of Lille in 1990. Since then, he has been professor at the University of Valenciennes. He is leader of the “Mobile & Embedded Systems" research group at the “Laboratory For Automation, Mechanical and Computer Engineering”, a joint research unit between CNRS and the university of Valenciennes.

S.Niar co-supervises the «Intelligent infrastructures & vehicles » task within the International Campus on Safety and Inter-modality in Transportation (“Campus International sur la Sécurité l’Intermodalité dans les Transports” CISIT) in Valenciennes. He has been research associate at INRIA-Futurs from 2004 till 2011.

Prof. S.Niar is member of the editorial board at the “Embedded Hardware Design: Microprocessors and Microsystems” (Elsevier) journal and guest editor of a special issue on "Reliability and Dependability in new SoC Technologies".

He is member of the European Network of Excellence on “HIgh Performance and Embedded Architectures and Compilation” (HIPEAC). He was general chair of the Euromicro Digital System Design conference in 2010 (DSD’10) and program chair for the same conference in 2012. He was Co-Chair of the “Rapid Simulation and Performance Evaluation: Methods and Tools” (RAPIDO) workshops from 2009 up to 2012. The RAPIDO workshops have been organized every year in conjunction with the HIPEAC conference.

He also served as program chair, general chair or on program committees of several workshops, symposia and conferences in the domain of design tools for embedded systems and their applications. As expert for the FP7 European projects in Information and Communication Technologies (ICT) and expert for the French National Research Agency (Agence Nationale de la Recherche ANR), he reviewed several projects in the same domain.